ARCHITECTURES NUMÉRIQUES DE TRAITEMENT DE L'INFORMATION

DIGITAL ARCHITECTURES FOR COMPUTING AND INFORMATION PROCESSING

Lecturers: Ian O CONNOR

| Lecturers : 18 | TC : 10.0 | PW : 8.0 | Autonomy : 12 | Study : 0.0 | Project : 0.0 | Language : MI

Objectives

This course aims to study the hardware operation of digital electronic architectures for computing and information processing. It presents the components that are systematically present in digital architectures: control, data path and memory. The first part of the course will analyze the internal architecture of processors and the way in which they execute software instructions. The second part will focus on how (through the organization of the components) it is possible to improve the performance of the processor.

Keywords : Processors, datapath, software instructions, memory, pipeline architectures, cache memory

Programme

Architectural principles: von Neumann and (modified) Harvard, RISC, CISC
Datapath design, control and instruction flow
Instruction sets, memory, addressing types
Computing machine benchmarking.
Performance acceleration techniques: Pipeline, Cache memory

Learning outcomes

- Understand how a processor works
- Understand how processor hardware is programmed
- Understand the main performance metrics and parameters of architectures (memory footprint, speed, energy consumption)
- Know the main techniques to accelerate processor performance

Independent study

Objectifs : This activity is not concerned with framed autonomy activities outside personal work.

Méhodes : This activity is not concerned with framed autonomy activities outside personal work.

Core texts

John L. Hennessy, David A. Patterson, Morgan Kaufman, *COMPUTER ARCHITECTURE: A QUANTITATIVE APPROACH* , 2006
David A. Patterson, John L. Hennessy, Morgan Kaufman *COMPUTER ORGANIZATION AND DESIGN: THE HARDWARE/SOFTWARE INTERFACE* , 2008
David Harris, Sarah Harris*DIGITAL DESIGN AND COMPUTER ARCHITECTURE* , 2007

Assessment

Final mark = 50% Knowledge + 50% Know-how
Knowledge mark = 100% final exam
Know-how mark = 50% TP1 report + 50%TP2 report